AMENDMENTS TO THE SPECIFICATION

Amend the paragraph beginning at page 1, line 3 as follows:

[[* * * *]]

Amend the paragraph beginning at page 1, line 4 as follows:

~~DESCRIPTION~~

Insert the following heading and paragraph beginning at page 1, line 4:

Related Application:

The present application is a U.S. national filing and claims priority of PCT/EP2005/050737 filed February 21, 2005, which claims priority of Italian Patent Application No. MI2004A000383 filed March 2, 2004, both of which applications are incorporated herein in their entireties by this reference.

Insert the following heading at page 1, line 5:

Field of the Invention:

Insert the following heading and amend the paragraph beginning at page 1, line 11:

Background:

[[These]] Network converters such as those described above, are fitted with a transformer and a switch (typically MOSFET) that periodically connects a transformer winding to the input source, that is to a network voltage rectified by a diode bridge and filtered by a capacitor.

Amend the paragraph beginning at page 4, line 3 as follows:

This is mainly due to the parasitic parameters of the transformer, by effect of which with high load the voltage rises far more than scheduled by effect of the peaks present on the positive fronts of the voltage on Wa, while with low or [[nil]] negligible load, where the peaks are much lower and the load on Wa is represented by the integrated control circuit 12, can also be greater than that in output, the voltage diminishes considerably below the expected value.

Amend the paragraph beginning at page 4, line 6 as follows:

In the more modern integrated control circuits 12, this is accentuated by the adoption of several special techniques aimed at minimizing the consumptions of the power supply at low loads so as to facilitate compliance with the most recent regulations regarding the reduction of consumption of equipment in non-operative conditions (for example EnergyStar, Energy2000, Blue Angel, etc.). These techniques basically entail the reduction of the operative frequency of the power supply at minimum or [[nil]] negligible loads; therefore the energy that Wa is capable of transferring is diminished.

Amend the paragraph beginning at page 4 line, 14 as follows:

Another problem is represented by the fact that the voltage Vcc cannot exceed a determined value Vccmax for questions linked to the technology of the integrated control circuit 12 that impose limits to the voltage applicable to it and, at the same time, in conditions of minimum or [[nil]] negligible load, Vcc has to stay greater than Vstop, otherwise the system will function intermittently. The variations of the voltage generated by Wa [[must]] are therefore limited, with some margin of safety, within the interval Vstop - Vccmax.

Amend the paragraph beginning at page 4 line, 24 as follows:

To limit the phenomenon of over-high voltage at maximum load and to ensure intermittent operation in short circuit conditions, as well as optimising the constructive methods of the transformer, generally the resistance Rr is used in series with the diode D with the purpose of smoothing the peaks. Sometimes, as an alternative, a small inductor is used. However, both solutions accentuate the decrease of Vcc at minimum or [[nil]] negligible loads. Also optimising the value of this resistor or inductor (that is, using the minimum value) so as to ensure functioning in safe conditions both at maximum load ($Vcc<Vccmax$) and in short circuit ($Vcc<Vstop$), it is difficult to fulfil the condition $Vcc>Vstop$ at minimum or [[nil]] negligible load. To resolve this latter problem a ballast load is added to the power supply so as to contrast the decrease of Vcc. This, however, worsens the efficiency of the system and, above all, makes it practically impossible to comply with the various EnergyStar, Energy2000, Blue Angel, etc.

Amend the paragraph beginning at page 5, line 8 as follows:

The same also goes for other external circuitry solutions intended for minimizing the effect of the peaks. In all, meeting the conditions $Vcc <Vccmax$ at full load and Vcc

< Vstop in short circuit, makes it extremely difficult to also fulfil the condition Vcc > Vstop at minimum or [[nil]] negligible load.

Amend the paragraph beginning at page 6, line 2 as follows:

This system effectively stabilizes the Vcc starting from low loads up to full load and ensures that the condition Vcc<Vstop in short circuit for the converter can be easily obtained. At very low or [[nil]] negligible load, however, it cannot keep the Vcc stable, that decreases considerably, worse than in the case of the circuit of Figure 1. In fact, the transistor T introduces an additional fall of voltage (Vcesat) and, above all, masks partially or completely the horizontal section of the voltage of Waux which is very short. On the contrary to what happens at full load, in these conditions the pulses, even though being small, would give a small addition of energy capable of obstructing, at least partially, the tendency of Vcc to decrease.

Insert the following heading at page 6, line 12:

SUMMARY OF THE INVENTION

Amend the paragraph beginning at page 6, line 25 as follows:

This object is also achieved by means of a switching power supply comprising a circuit for reducing the variations of the auto-supply voltage of the control circuit of a switching power supply ~~in accordance with claim 1.~~ including a generator of said auto-supply voltage, a controlled switch capable of selectively coupling said generator to said control circuit, and a driving circuit of said controlled switch that supplies a closing signal of said controlled switch after a predefined time delay starting from said deactivation command.

Amend the paragraph beginning at page 7, line 5 as follows:

~~Thanks~~ According to the present invention it is possible to produce a circuit capable of minimizing the variations of the auto-supply voltage of control circuits that guarantees safety in functioning in short-circuit conditions (Vcc < Vstop), that facilitates achieving compliance to the regulations regarding consumption of equipment at minimum or [[nil]] negligible load (Vcc > Vstop), that simplifies the construction of the transformer and of the auxiliary winding, and is capable of protecting from overloads in output, that is, capable of turning off the converter when the overload lasts longer than a predefined

time.

Insert the following heading at page 7, line 14:

BRIEF DESCRIPTION OF THE DRAWINGS

Amend the paragraph beginning at page 7, line 26 as follows:

Figure 5 shows a possible embodiment of the block diagram of Figure 3; and

Amend the paragraph beginning at page 7, line 28 as follows:

Figure 6 shows in a diagram the results of the performances of the circuits of ~~Figure~~ Figures 1, 2 and 5.

Insert the following heading at page 7, line 30:

DETAILED DESCRIPTION

Amend the paragraph beginning at page 8, line 26 as follows:

The object of the circuit of Figure 3 is to drive the switch SW, placed in series to the auxiliary winding Wa, in opposition of phase with the power transistor TP and delaying its turn-on, in relation to the turn-off of the power transistor TP itself, by a time subject to a representative signal of the load conditions of the converter so that said delay is minimum or [[nil]] negligible when the above-mentioned signal indicates a load lower than a predefined value Vt1 and that assumes suitable values so as to mask the pulses of Wa when the abovementioned signal indicates a load greater than said value.

Amend the paragraph beginning at page 9, line 21 as follows:

In regard to the practical implementation, it would be better if this were carried out inside the integrated control circuit. In principle the integration could be total, that is, the switch SW could also be integrated. In this case several problems arise. Two available pins of the device are needed, one to connect to an end of the winding Wa and the other, which would be the pin supplying the chip, would be connected to the capacitor Cs. The pin to connect to Wa can also take on a voltage of several tens of negative volts in relation to ground, therefore either it is necessary for the pin to be structured so as to support these heavy negative voltages or a diode (with cathode turned towards the pin) has to be interposed that insulates the pin when the voltage on Wa is negative. The current that

flows through SW is the impulse type; even though its average value does not go over several mA, it flows for a rather small fraction of the cycle so the impulse value can also be much greater. It follows then that SW [[must]] should be capable of supporting the impulse current with a minimum fall of voltage and its dimensions could be anything but insignificant.

Amend the paragraph beginning at page 10, line 23 as follows:

The relation between the introduced delay in turn-on Td and Vcomp can be of any type as long as Td is minimum or [[nil]] negligible at low load, that is when Vcomp is lower than a threshold Vt1. Optionally the turn-on of SW2 could be inhibited in overload conditions, that is when Vcomp is higher than a threshold Vt2. In the interval Vt1-Vt2, Td can be constant or, more generally, non-digressive function of V(COMP).